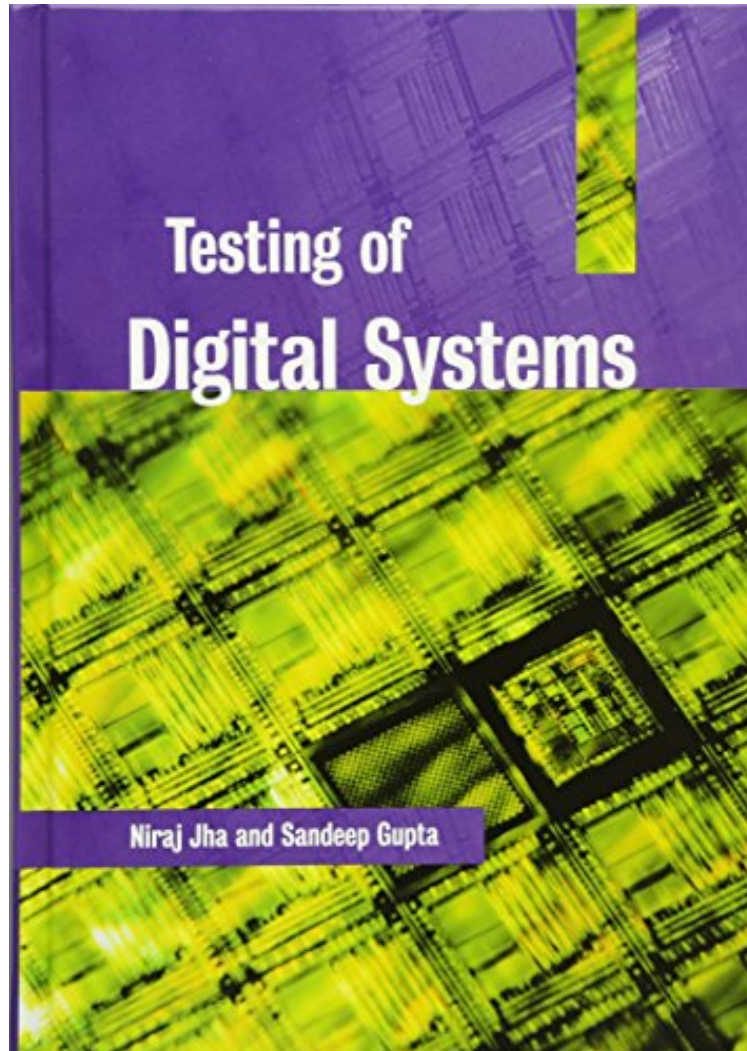


# Testing of Digital Systems

*N. K. Jha, S. Gupta*

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#2310742 in Books Cambridge University Press 2003-05-15 Original language: English PDF # 1 9.72 x 1.93 x 6.851, 4.80 #File Name: 05217735631016 pages | File size: 26.Mb

**N. K. Jha, S. Gupta : Testing of Digital Systems** before purchasing it in order to gage whether or not it would be worth my time, and all praised Testing of Digital Systems:

7 of 11 people found the following review helpful. Difficult to UnderstandBy AaronI starting reading this book with an open mind and thought I would like it. However, after the first chapter I began encountering unexplained notation and abbreviations that do not exist in the index. I have started finding many algorithms and concepts that leave me scratching my head - either the authors are brilliant or they've managed to pull together an impressive array of equations and explanations from research papers in an utterly incomprehensible manner (perhaps too much is crammed into one book?). My professor seems to love the notations and explanations, so maybe it's just me. Also, I don't

understand why the authors need to introduce box symbols for digital gates (AND, NAND, etc.) when easily recognizable symbols already exist in the industry.

Device testing represents the single largest manufacturing expense in the semiconductor industry, costing over \$40 billion a year. The most comprehensive and wide-ranging book of its kind, *Testing of Digital Systems* covers everything you need to know about this vitally important subject. Starting right from the basics, the authors take the reader through every key area, including detailed treatment of the latest techniques such as system-on-a-chip and IDDQ testing. Written for students and engineers, it is both an excellent senior/graduate level textbook and a valuable reference.

About the Author Niraj Jha is Professor of Electrical Engineering at Princeton University and head of the Center of Embedded System-on-a-Chip Design, where his current research is focussed on the synthesis and testing of these devices. He is a fellow of IEEE, associate editor of IEEE Transactions on VLSI Systems and The Journal of Electronic Testing: Theory and Applications (JETTA) and a recipient of the ATT Foundation award and the NEC preceptorship award for research excellence. Sandeep Gupta is an Associate Professor in the Department of Electrical Engineering at the University of Southern California, USA. He is Co-Director of the M.S. Program in VLSI Design, with research interests in the area of VLSI testing and design. He is a member of the IEEE.